PROGRAMMABLE INTERRUPT CONTROLLER 8259A

The processor 8085 had five hardware interrupt pins. Out of these five interrupt pins, four pins were allotted fixed vector addresses but the pin INTR was not allotted any vector address, rather an external device was supposed to hand over the type of the interrupt, i.e. (Type 0 to 7 for RST0 to RST7), to the microprocessor. The microprocessor then gets this type and derives the interrupt vector address from that. Consider an application, where a number of I/O devices connected with a CPU desire to transfer data using interrupt driven data transfer mode. In these types of applications, more number of interrupt pins are required than available in a typical microprocessor. Moreover, in these multiple interrupt systems, the processor will have to take care of the priorities for the interrupts, simultaneously occur· ring at the interrupt request pins. To overcome all these difficulties, we require a programmable interrupt controller which is able to handle a number of interrupts at a time. This controller takes care of a number of simultaneously appearing interrupt requests along with their types and priorities. This will relieve the processor from all these tasks. The programmable interrupt controller 8259A from Intel is one such device. The predecessor 8259 was designed to operate only with 8-bit processors like 8085. A modified version, 8259A was later introduced that is compatible with 8-bit as well as 16-bit processors.

Architecture and Signal Descriptions of 8259A

The architectural block diagram of 8259A is shown in Fig. 1.1. The functional explanation of each block is given in the following text in brief.

Interrupt Request Register (IRR)

The interrupts at IRQ input lines are handled by Interrupt Request Register internally. IRR stores all the interrupt requests in it in order to serve them one by one on the priority basis.The IRR has eight input lines(IR0-IR7) for intrrupts.When these lines go high ,the request are stored in the IRR.Normally IR0 has the highest priority and IR7 the lowest. The priorities of an interrupt request input are also programmable.

In-Service Register (ISR)

This stores all the interrupt requests those are being served, i.e ISR keeps a track of which interrupt input is currently being served. For each input that is currently serviced ,the corresponding bit will be set in the in service register

Priority Resolver

This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during INTA pulse. The IR0 has the highest priority while the IR7 has the lowest one, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode.

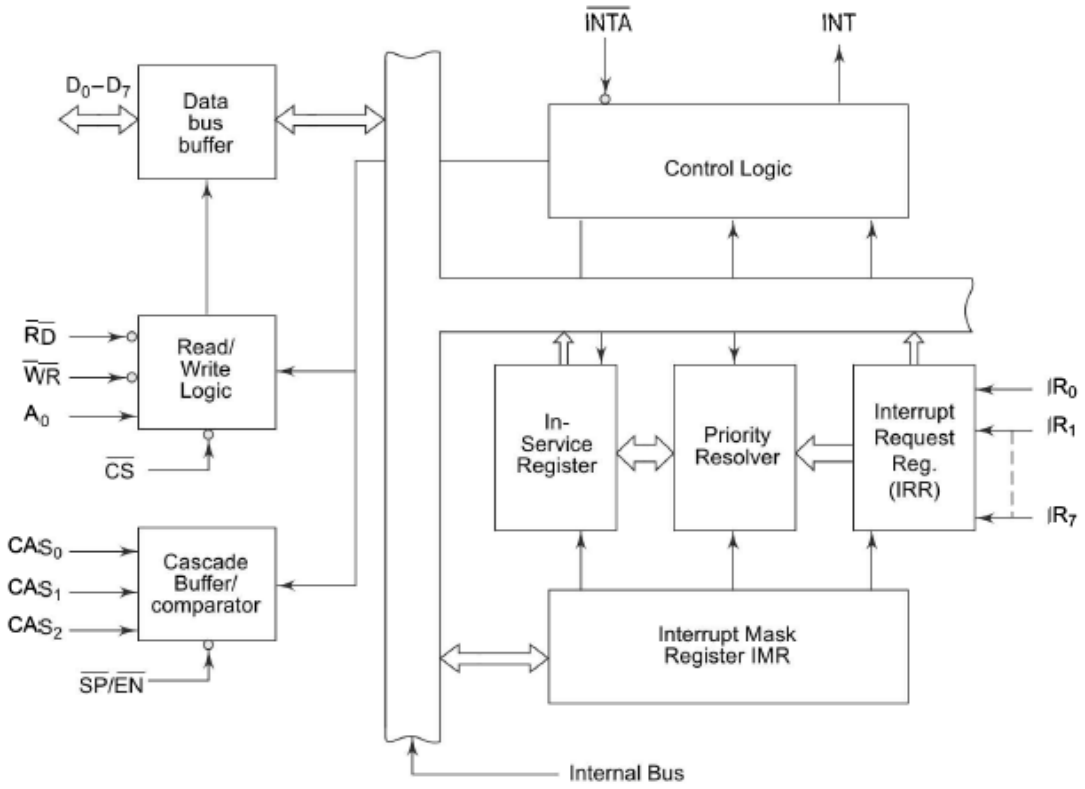


Fig1.1. 8259A Block Diagram

Interrupt Mask Register (IMR)

This register stores the bits required to mask the interrupt puts. IMR operates on IRR at the direction of the Priority Resolver.The relevant information is sent by the processor through OCW1

Interrupt Control Logic

This block manages the interrupt and interrupt acknowledge sigD8ls to be sent to the CPU for serving one of the eight interrupt requests. This also accepts interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus.

Data Bus Buffer

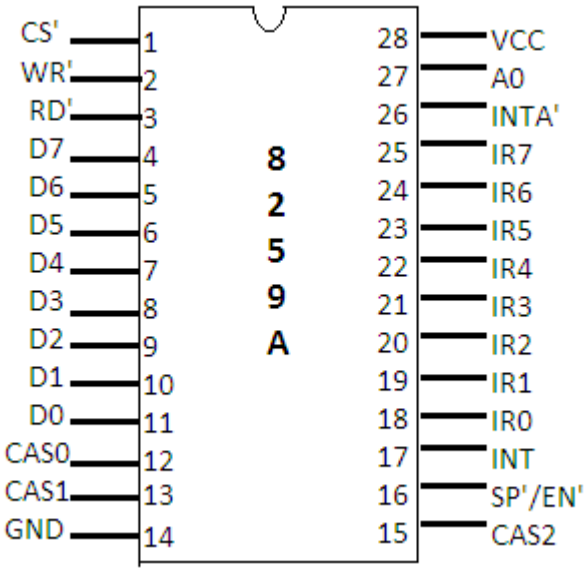
This tristate bidirectional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through buffer during read or write operations.

Read write Control Logic

This circuit accepts and decodes commands from the CPU. This also allows the status of the 8259A to be transferred on to the data bus.

Cascade Buffer/Comparator

This block stores and compares the ID's of all the 8259As used in the system. The three I/O pins CAS0-2 are outputs when the 8259A is used as a master. The same pins act as inputs when the 8259A is in slave mode. The 8259A in master mode sends the ID of the interrupting slave device on these lines. The slave thus selected, will send its pre programmed vector address on the data bus during the next INTA pulse.
Figure 1.2 shows the pin configuration of 8259A, followed by their functional description of each of the signals in brief.



CS

This is an active-low chip select signal for enabling RD* and WR* operations of 8259A.INTA* function is independent of CS*.

WR*

This pin is an active-low write enable input to 8259A. This enables it to accept command words from CPU.

RD*

This is an active-low read enable input to 8259A. A low on this line enables 8259A to release status onto the data bus of CPU. D7-D0 These pins form a bidirectional data bus that carries 8-bit data either to control word or from status word registers. This also carries interrupt vector information.

CASo-CAS2

Cascade Lines A single 8259A provides eight vectored interrupts. If more interrupts are required, the 8259A is used in cascade mode. In cascade mode, a master 8259A along with eight slaves 8259A can provide up to 64 vectored interrupt lines. These three lines act as select lines for addressing the slaves 8259A.

PS*/EN*

This pin is a dual purpose pin. When the chip is used in buffered mode, it can be used as buffer enable to control buffer transreceivers. If this is not used in buffered mode then the pin is used as input to designate whether the chip is used as a master (SP = 1) or a slave (EN = 0).

INT

This pin goes high whenever a valid interrupt request is asserted. This is used to interrupt the CPU and is connected to the interrupt input of CPU.

IR0-IR7(1nterrupt requests)

These pins act as inputs to accept interrupt requests to the CPU. In edge triggered mode, an interrupt service is requested by raising an IR pin from a low to a high state and holding it high until it is acknowledged, and just by latching it to high level, if used in level triggered mode.

INTA* (Interrupt acknowledge)

This pin is an input used to strobe-in 8259A interrupt vector data on to the data bus. In conjunction with CS, WR, and RD pins, this selects the different operations like, writing command words, reading status word, etc.

The device 8259A can be interfaced with any CPU using either polling or interrupt. In polling, the CPU keeps on checking each peripheral device in sequence to ascertain if it requires any service from the CPU. If any such service request is noticed, the CPU serves the request and then goes on to the next device in sequence. After all the peripheral devices are scanned as above the CPU again starts from the first device. This type of system operation results in the reduction of processing speed because most of the CPU time is consumed in polling the peripheral devices.

In the interrupt driven method, the CPU performs the main processing task till it is interrupted by a service requesting peripheral device. The net processing speed of these type of systems is high because the CPU serves the peripheral only if it receives the interrupt request. If more than one interrupt requests are received at a time, all the requesting peripherals are served one by one on priority basis. This method of interfacing may require additional hardware if number of peripherals to be interfaced is more than the interrupt pins available with the CPU.

Interrupt Sequence in an 8086 System

The interrupt sequence in an 8086-8259A system is described as follows:

First the 8259 should be programmed by sending the initialization command word(ICW) and the operational command word(OCW)

Once the 8259 is programmed, it is ready for accepting interrupt signal

1. When it receives an interrupt through any one of the interrupt lines (IR0-IR7) it checks for its priority
2. 8259A resolves priority and sends an INT signal to the INTR pin of the 8086

3. The CPU acknowledges with INTA pulse. When the processor accepts the interrupt it sends two INTA one by one .The first INTA is set to 8259 to inform the acceptance of the interrupt and to prepare the 8259 for supplying the type number The second INTA is sent to to the 8259 to read the type number from 8259
4. Upon receiving an INTA signal from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive data bus during this period.
5. The 8086 will initiate a second INTA pulse. During this period 8259A releases an 8-bit pointer on to data bus from where it is read by the CPU.
6. This completes the interrupt cycle. The ISR bit is reset at the end of the second INTA pulse if automatic end of interrupt (AEOI) mode is programmed. Otherwise ISR bit remains set until an appropriate EOI command is issued at the end of interrupt subroutine.

Command Words of 8259A

The command words of 8259A are classified in two groups, viz**. initialization command words** (ICWs) and **operation command words** (OCWs)Initialization Command Words (ICWs) Before it starts functioning, the 8259A must be initialized by writing two to four command words into the respective command word registers. These are called as initialization command words (ICWs). If A0 = 0 and D4 = 1, the control word is recognized as ICW1 It contains the control bits for edge/level triggered mode, single/cascade mode, call address interval and whether ICW4 is required or not, etc. If A0 = 1, the control word is recognized as ICW2. The ICW2 stores details regarding interrupt vector addresses. The initialization sequence of 8259A is described in from of a flow chart in Fig. 1.3. The bit functions of the ICW1 and ICW2 are self explanatory as shown in Fig. 1.4.

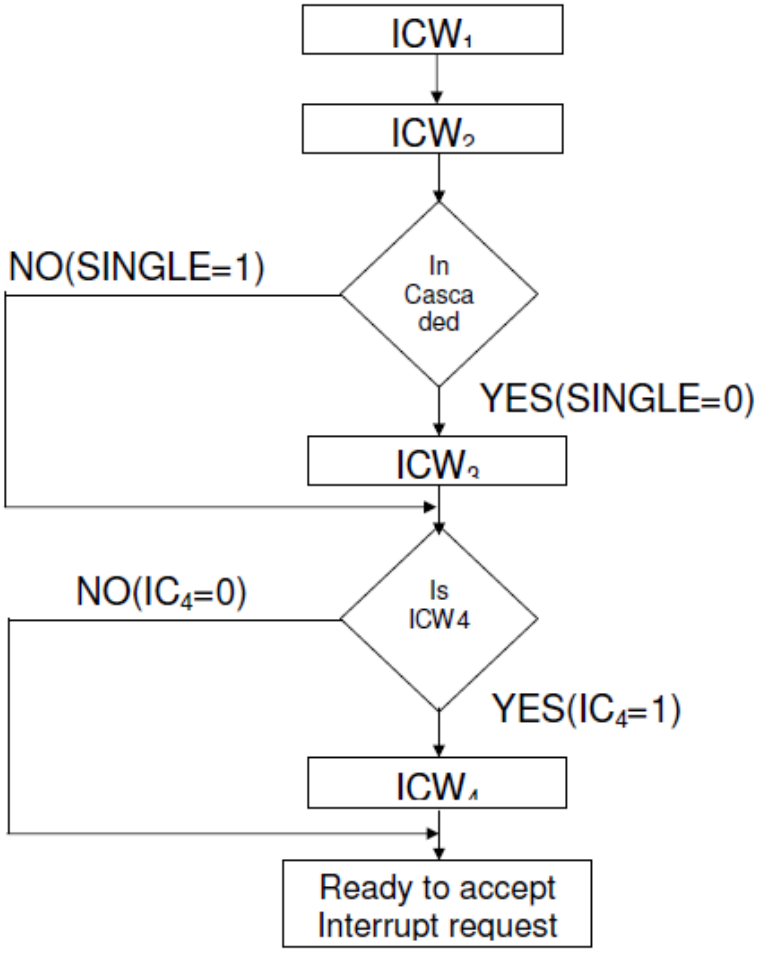


Fig1.3. Initialisation Sequence of 8259A

Once ICW1 is loaded, the following initialization procedure is carried out internally.

(a) The edge sense circuit is reset, i.e. by default 8259A interrupts are edge sensitive.

(b) IMR is cleared.

(c) IR7 input is assigned the lowest priority.

(d) Slave mode address is set to 7.

(e) Special mask mode is cleared and status read is set to IRR.

(f) If IC4 = 0, all the functions of ICW4 are set to zero. Master/slave bit in ICW4 is used in the buffered mode only.

In an 8085 based system, A15 – A8 of the interrupt vector address are the respective bits of ICW2. In 8086/88 based system A15 – A11 of the interrupt vector address are inserted in place of T7 - T3 respectively and the remaining three bits (A8, A9 and A10) are selected depending upon the interrupt level, i.e. from 000 to 111 for IR0 to IR7.

ICW1 and ICW2 are compulsory command words in initialization sequence of 8259A as is evident from Fig. 1.3, while ICW3 and ICW4 are optional. The ICW3 is read only when there are more than one 8259As in the system, i.e. cascading is used (SNGL = 0). The SNGL bit in ICW1 indicates whether the 8259A is in cascade mode or not. The ICW3 loads an 8-bit slave register. Its detailed functions are as follows.

In master mode [i.e. SP = 1 or in buffer mode M/S = 1 in ICW4], the 8-bit slave register will be set bit-wise to '1' for each slave in the system, as shown in Fig. 1.5. The requesting slave will then release the second byte of a CALL sequence.

In slave mode [i.e.SP=0 or if BUF=1 and M/S=0 in ICW4] bits D2 to D0 identify the slave, i.e 000 to 111 for slave 1 to slave 8. The slave compares the cascade inputs with these bits and if they are equal, the second byte if the CALL sequence is released by it on the data bus.

ICW_1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LITM	ADI	SNGL	IC_4

D_0 1=ICW_4 Needed
0=No ICW_4 Needed

D_1 1=Single
0=Cascaded

D_2 Call Address Interval
1=Interval of 4 bytes
0=Interval of 8 bytes

D_3 1=Level Triggered
0=Edge Triggered

A_7-A_5 of Interrupt vector address
MCs 80/85 mode only

ICW_2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	T_7	T_6	T_5	T_4	T_3	A_{10}	A_9	A_8

T_7-T_3 are $A_3 - A_0$ of Interrupt vector address
$A_{10} - A_9$, A_8 – Selected according to Interrupt request level.
They are not the address lines to microprocessor
A_0 – 1 Selects ICW_2

Fig1.4. Initialisation Command Words ICW_1 and ICW_2

Master ICW_3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

$S_n = 1 - IR_n$ Input has a slave
$=0 - IR_n$ Input does not have a slave

Slave ICW_4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

$D_2\ D_1\ D_0$ – 000 to 111 for IR_0 to IR_7 or slave 1 to slave 8

Fig1.5. ICW_3 in Master and Slave Mode

ICW4 The use of this command word depends on the IC4 bit of ICW1. If IC4= 1, ICW4 is used, otherwise it is neglected. The bit functions of ICW4 are described as follows:

SFNM Special fully nested mode is selected, if SFNM = 1.
BUF If BUF = 1, the buffered mode is selected. In the buffered mode,SP/EN acts as enable output and the master/slave is determined using the M/S bit of ICW4.
M/S If M/S = 1, 8259A is a master. If M/S = 0, 8259A is a slave. If BUF =0, M/S is to be neglected.
AEOI If AEOI = 1, the automatic end of interrupt mode is selected.

µPM If the µPM bit is 0, the Mcs-85 system operation is selected and if/µPM =1, 8086/88 operation is selected.

ICW_4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SFNM	BUF	M/S	AEOI	µPM

Fig1.6 shows the ICW_4 bit positions

Operation Command Words(OCW)

Once 8259A is initialized using the previously discussed command words for initialisation, it is ready for its normal function, i.e. for accepting the interrupts but 8259A has its own ways of handling the received interrupts called as modes of operation. These modes of operations can be selected by programming, i.e. writing three internal registers called as operation command word registers. The data written into them (bit pattern) is called as operation command words. In the three operation command words OCWl ,OCW2 and OCW3 every bit corresponds to some operational feature of the mode selected, except for a few bits those are either '1' or '0'. The three operation command words are shown in Fig. 1.7 (a), (b) and (c) with the bit selection details. OCW1 is used to mask the unwanted interrupt requests. If the mask bit is '1', the corresponding interrupt request is masked, and if it is '0', the request is enabled. In OCW2 the three bits, viz. R, SL and EOI control the end of interrupt, the rotate mode and their combinations as shown in Fig. 1.7

(b), The three bits L2, L1 and L0 in OCW2 determine the interrupt level to be selected for operation , if the SL bit is active, i.e. '1'. The details of OCW2 are shown in Fig. 1.7(b).

In operation command word 3 (OCW3), if the ESMM bit, i.e. enable special mask mode bit is set to '1', the SMM bit is enabled to select or mask the special mask mode. When ESMM bit is '0', the SMM bit is neglected. If the SMM bit, i.e.special mask mode bit is '1', the 8259A will enter special mask mode provided ESMM = 1.

If ESMM = 1 and SMM = 0, the 8259A will return to the normal mask mode. The details of bits of OCW3 are given in Fig. 1.7 (c) along with their bit definitions.

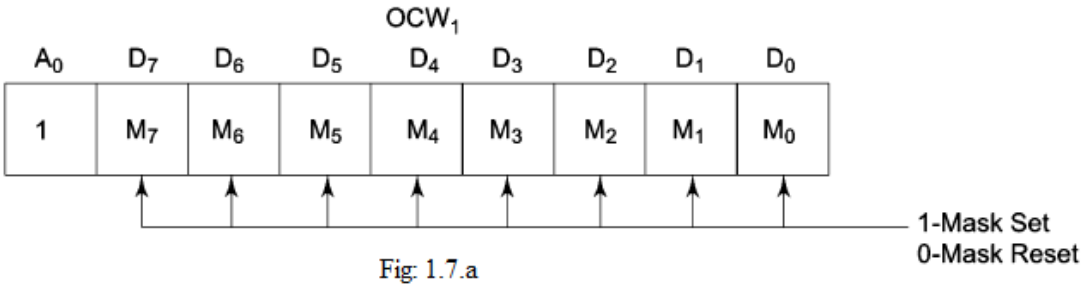


Fig: 1.7.a

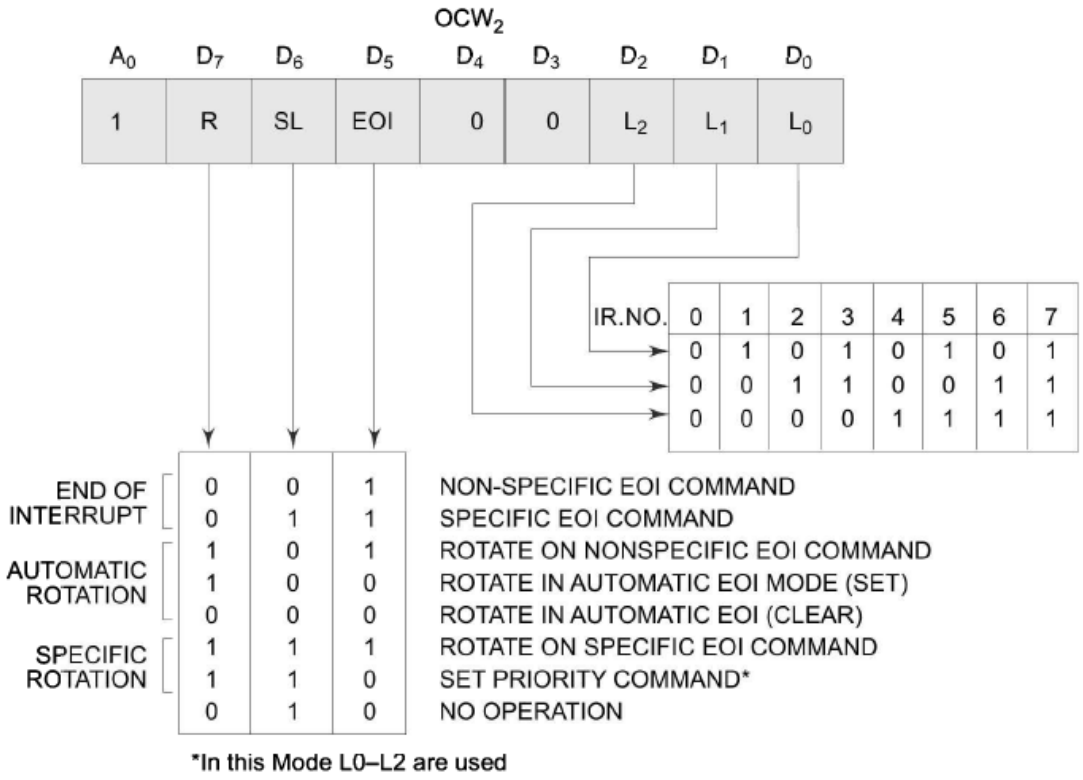
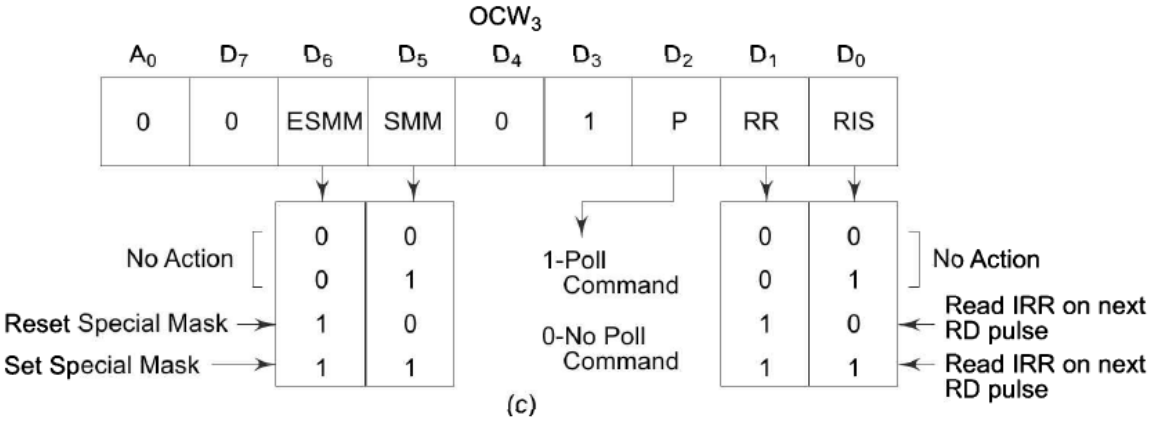


Fig.1.7.b



(c)

Fig.1.7.c

Operating Modes of 8259

The different modes of operation of 8259A can be programmed by setting or resting the appropriate bits of the ICWs or OCWs as discussed previously. The different modes of opera· tion of 8259A are explained in the following text.

Fully Nested Mode

This is the default mode of operation of 8259A. IR0 has the highest priority and IR7 has the lowest one. When interrupt requests are noticed,the highest priority request amongst them is determined and the vector is placed on the data bus. The corresponding bit of ISR is set and remains set till the microprocessor issues an EOI command just before returning from the service routine or the AEOI bit is set. If the ISR (in service) bit is set, all the same or lower priority interrupts are inhibited but higher levels will generate an interrupt, that will be acknowledged only if the microprocessor's interrupt enable flag (IF) is set. The priorities can afterwards be changed by programming the rotating priority modes.

End of Interrupt (EOI)

The ISR bit can be reset either with AEOI bit of ICW1 or by EOI command, issued before returning from the interrupt service routine. There are two types of EOI commands specific and non-specific. When 8259A is operated in the modes that preserve fully nested structure, it can determine which ISR bit is to be reset on EOT. When nonspecific EOI command is issued to 8259A it will automatically reset the highest ISR bit out of those already set. When a mode that may disturb the fully nested structure is used, the 8259A is no longer able to determine the last level acknowledged. In this case a specific EOI command is issued to reset a particular ISR bit. An ISR bit that is masked by the corresponding IMR bit, will not be cleared by a non-specific EOI of 8259A, if it is in special mask mode.

Automatic Rotation

This is used in the applications where all the interrupting devices are of equal priority. In this mode, an interrupt request (IR) level receives lowest priority after it is served while the next device to be served gets the highest priority in sequence. Once all the devices are served like this, the first device again receives highest priority.

Automatic EOI Mode

Till AEOI = 1 in ICW4, the 8259A operates in AEOI mode. In this mode, the 8259A performs a non-specific EOI operation at the trailing edge of the last INTA pulse automatically. This mode should be used only when a nested multilevel interrupt structure is not required with a single 8259A.

Specific Rotation

In this mode a bottom priority level can be selected, using L2, L1 and L0 in OCW2 and R =1, SL = 1, EOI = 0. The selected bottom priority fixes other priorities. If IR5 is selected as a bottom priority, then IR5 will have least priority and IR4 will have a next higher priority. Thus IR6 will have the highest priority. These priorities can be changed during an EOI command by programming the rotate on specific EOI command in OCW2

Special Mask Mode

In special mask mode, when a mask bit is set in OCWl, it inhibits further interrupts at that level and enables interrupt from other levels, which are not masked.

Edge and Level Triggered Mode

This mode decides whether the interrupt should be edge triggered or level triggered. If bit LTIM of ICWl = 0, they are edge triggered, otherwise the interrupts are level triggered.Reading 8259 Status The status of the internal registers of 8259A can be read using this mode. The OCW3 is used to read IRR and ISR while OCWl is used to read IMR. Reading is possible only in no polled mode.

Poll Command

In polled mode of operation, the INT output of 8259A is neglected, though it functions normally, by not connecting INT output or by masking INT input of the microprocessor. The poll mode is entered by setting P =1 in OCW3. The 8259A is polled by using software execution by microprocessor instead of the requests on INT input. The 8259A treats the next RD pulse to the 8259A as an interrupt acknowledge. An appropriate ISR bit is set, if there is a request. The priority level is read and a data word is placed on to data bus, after RD is activated. The data word is shown in Fig. 1.8.

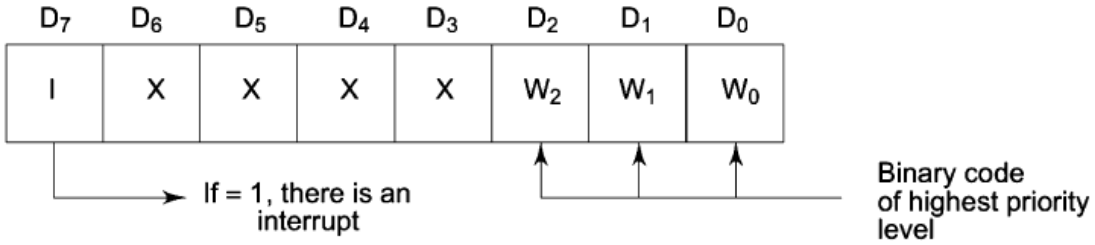


Fig.1.8

A poll command may give you more than 64 priority levels. Note that this has nothing to do with the 8086 interrupt structure and the interrupt priorities.

Special Fully Nested Mode

This mode is used in more complicated systems, where cascading is used and the priority has to be programmed in the master using ICW4. This is somewhat similar to the normal nested mode. In this mode, when an interrupt request from a certain lave is in service, this slave can further send requests to the master, if the requesting device connected to the slave has higher priority than the one being currently served. In this mode, the master interrupts the CPU only when the interrupting device has a higher or the same priority than the one currently being served. In normal mode, other requests than the one being served are masked out.When entering the interrupt service routine the software has to check whether this is the only request from the slave. This is done by sending a nonspecific EOI command to the slave and then reading its ISR and checking for zero. If its zero, a non-specific EOI can be sent to the master, otherwise no EOI should be sent. This mode is

important, since in the absence of this mode, the slave would interrupt the master only once and hence the priorities of the 'lave inputs would have been disturbed.

Buffered Mode

When the 8259A is used in the systems where bus driving buffers are used on data buses (e.g. cascade systems). The problem of enabling the buffers exists. The 8259A sends buffer enable signal on SP /EN pin, whenever data is placed on the bus.

Cascade Mode

The 8259A can be connected in a system containing one master and eight laves (maximum) to handle up to 64 priority levels. The master controls the slaves using CAS0-CAS2 which act as chip select inputs (encoded) for slaves. In this mode, the slave INT outputs are connected with master IR inputs. When a slave request line is activated and acknowledged, the master will enable the slave to release the vector address during second pulse of INTA sequence. The cascade lines are normally low and contain slave address codes from the trailing edge of the first INT A pulse to the trailing edge of the second INT A pulse. Each 8259A in the system must be separately initialized and programmed to work in different modes. The EOI command must be issued twice, one for master and the other for the slave. A separate address decoder is used to activate the chip select line of each 8259A. Figure 1.9 shows the details of the circuit connections of 8259As in cascade scheme.

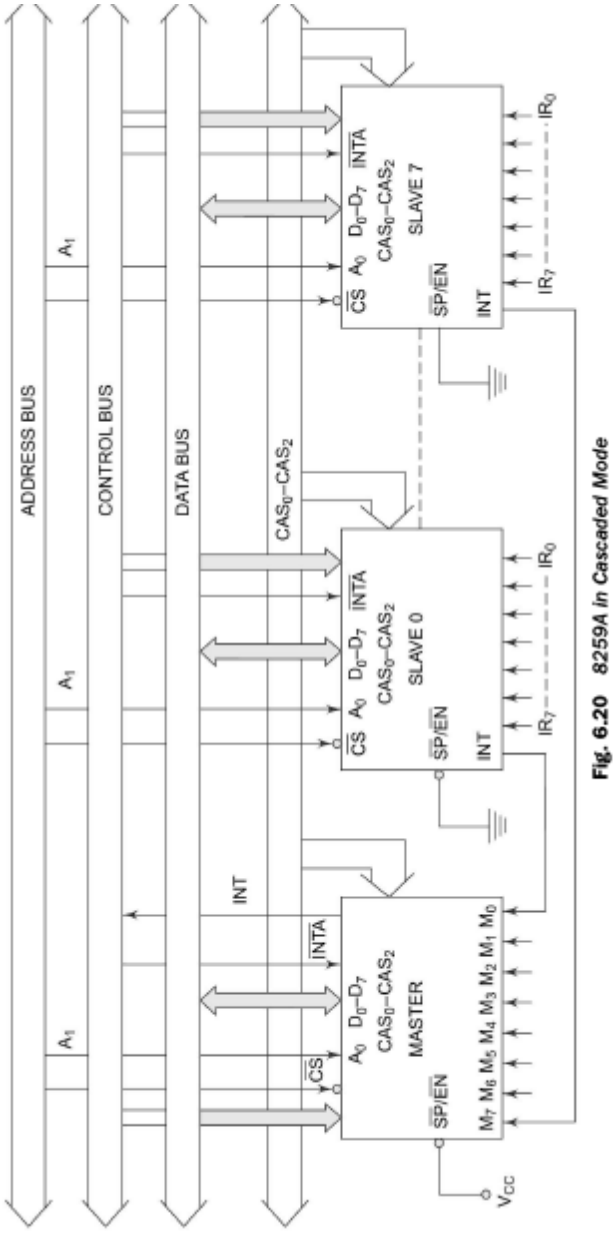
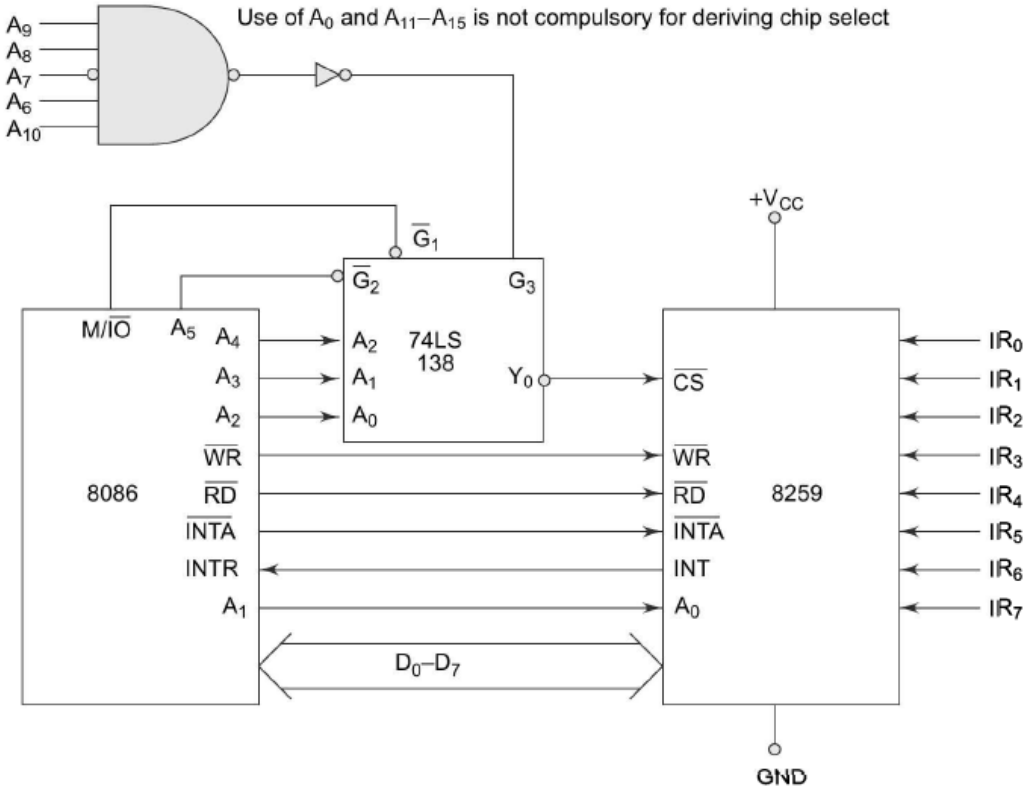


Fig. 6.20 *8259A in Cascaded Mode*

Interfacing and programming 8259



Example:

Show 8259A interfacing connections with 8086 at the address 074x. Write an ALP to initialize the 8259A in single level triggered mode. Then set the 8259A to operate with IR6 masked, IR4 as bottom priority level, with special EOI mode. Set special mask mode of 8259A. Read IRR and ISR into registers BH and BL respectively.

Solution:

Let the starting address is 0000:0010. The interconnections of 8259A with 8086 are as shown in Fig 1.10. The 8259 is interfaced with lower byte of the 8086 data bus, hence A0 line of the microprocessor system is abondened and A1 of the microprocessor system is connected with A0 of the 8259A. Before going for an ALP, all the initialisation command words (ICWS) and Operation command word (OCWS) must be decided. ICW1 decides single level triggered, address interval of 4 as given below.

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	1	1	1	1	1	= 1FH

D_0 ICW_4 Needed
D_1 Single 8259A
D_2 Call Address Interval 4
D_3 Level Triggered
D_4 Always set to 1
D_5 D_6 D_7 Don't care for 8086 system
A_0 Always set to 0

ICW_2 Vector address= 0000:0010 for IR_3

T7	T6	T5	T4	T3	A10	A9	A8	
1	0	0	0	0	0	1	1	=83H

A_8 A_9 A_{10} IR3 selected

There is no slave hence the ICW3 is as given below

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	0	ICW_3=00H

Actually ICW3 is not at all needed, because in ICW1 the 8259A is set for single mode.The ICW4 should be set as shown below:

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	1	ICW_4=01H

D0 For 8086 system
D1 Normal EOI
D2 D3 Non buffered mode
D4 For special fully nested mode masking

OCW1 Sets the mask of IR6 as shown below

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	0	0	0	0	0

OCW_1=40H

IR6 is masked

OCW2 Sets the modes and rotating priority as shown below

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	0	0	1	0	0

OCW_2=E4H

D0 D2 Bottom priority Level set at IR4D5 D7 Specific EOI Command with rotating priority

OCW3 Sets the special mask mode and reads ISR and IRR using the following control words.

For reading IRR

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	1	0	1	0

OCW_3=6AH

D0 D1 Read IRR
D2 No Poll command
D5 D7 Special mask mode

For reading ISR

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	1	0	1	1

OCW_3=6BH

D0 D1 Read ISR
D2 No Poll command
D5 D7 Special mask mode